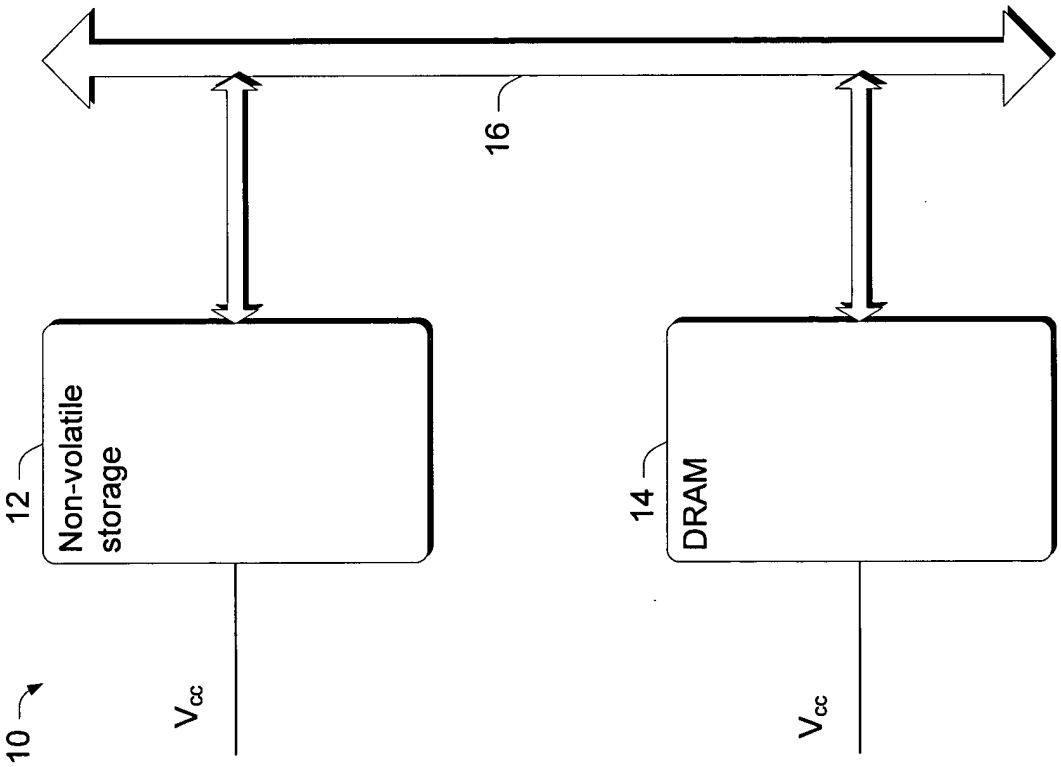

Fig. 1 (Prior Art)

Handling Object Store Page Exception

Exception Type	Current Access for OS page	Current Location of OS page	Action	Additional Notes
Write	Write	SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	DRAM or SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	Flash	(1) Copy the page into DRAM at physical address specified in the OS page table. (The faulting virtual address is used as a key into the OS page table in which the corresponding physical address is stored). (2) Modify the OS page table and TLB permissions for read-only accesses. (3) Copy the M bits to the F bits in order to specify where the page is located in flash in case of power loss. Modify the L bits to indicate that the page is now in DRAM. (4) Modify the SRAM object store page table M bits to specify the physical address in DRAM.	The access bits are changed to read only so that an attempt to write to the page will cause a write exception. In this exception handler, the page can be copied to SRAM before writing to it (thus making it dirty).

Fig.12A

Exception Type	Current Access for OS page	Current Location of OS page	Action	Additional Notes
Write or Read/write	Read	Flash	(1) Copy the page into SRAM at an available page slot. (2) Update the OS page table and the TLB physical address values to the page's address in SRAM. (3) Modify the OS page table and the TLB permissions for the access desired. (4) Modify the SRAM object store page table M bits to specify the physical address in SRAM. Modify the L bits to indicate that the page is now in SRAM. (5) Modify the SRAM page table, TLB, and OS page table access bits for the desired access.	The access bits are changed to read only so that an attempt to write to the page will cause a write exception. In this exception handler, the page can be copied to SRAM before writing to it (thus making it dirty).
Write or Read/write	Read	DRAM	See directly above	See directly above

Fig.12B